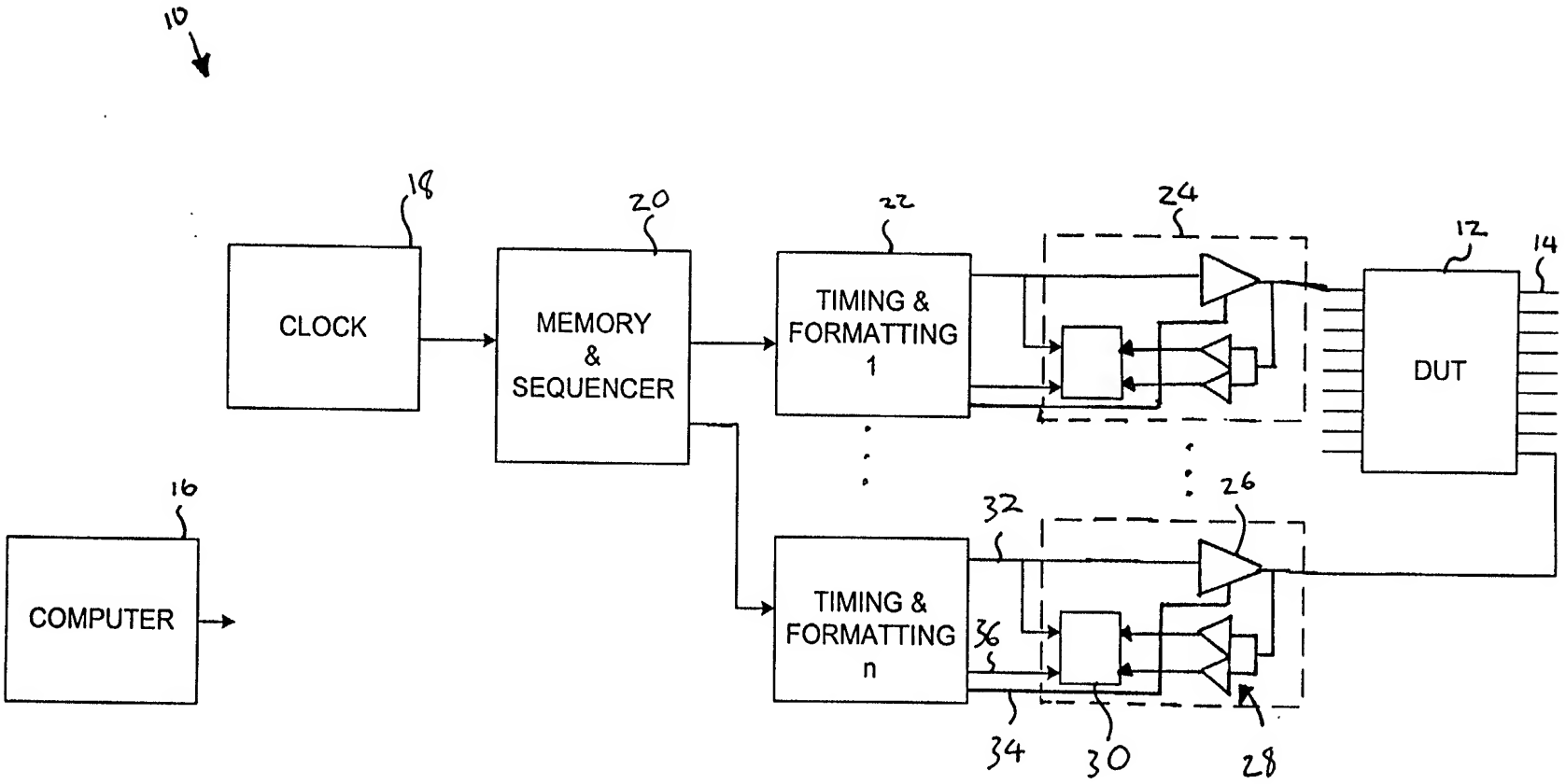

Fig. 1 (Prior Art)

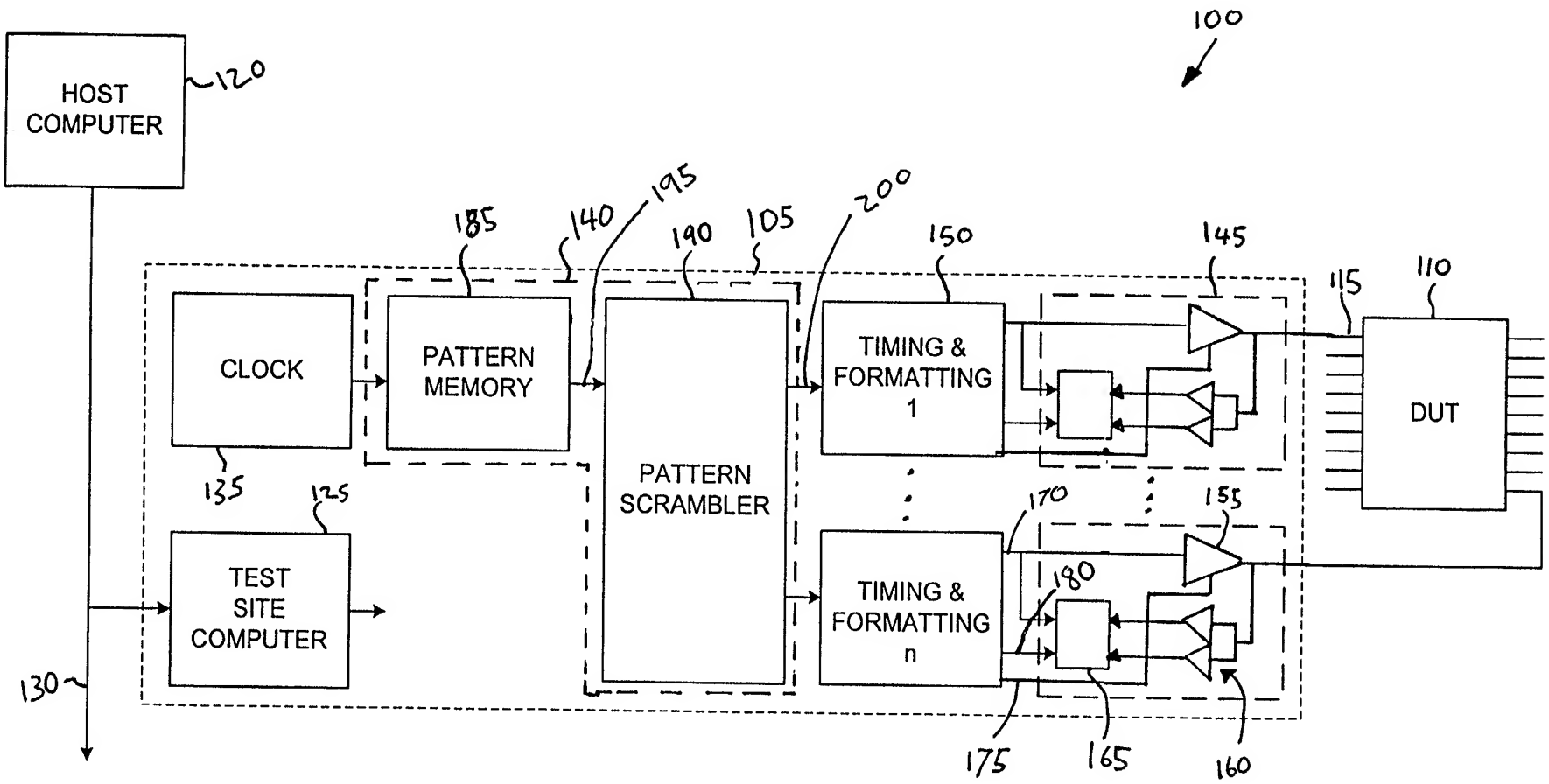

Fig. 2

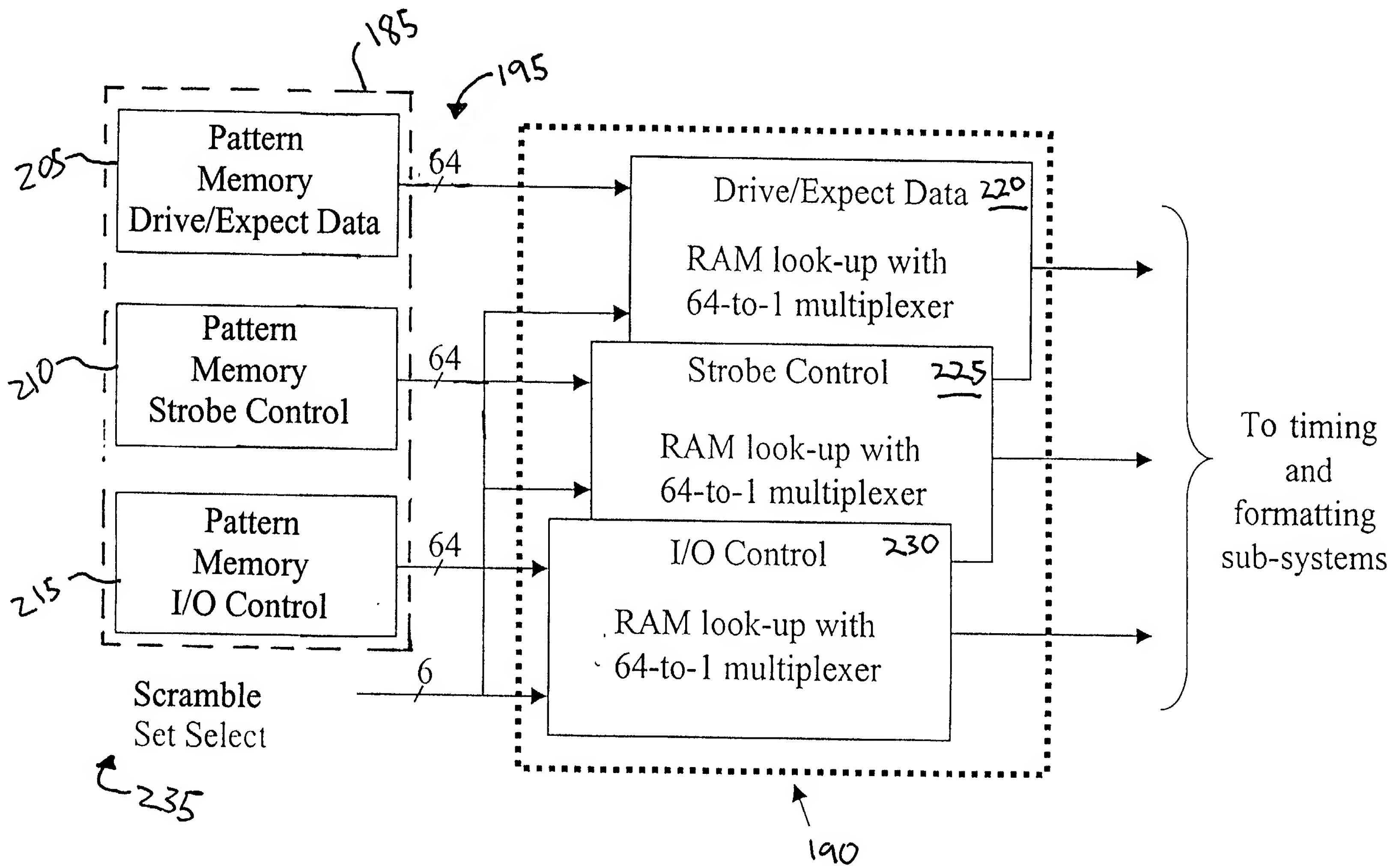
185
195
205
Pattern
Memory
Drive/Expect Data
210
Pattern
Memory
Strobe Control
215
Pattern
Memory
I/O Control
64
64
64
6
Scramble
Set Select
235
Drive/Expect Data 220
RAM look-up with
64-to-1 multiplexer
Strobe Control 225
RAM look-up with
64-to-1 multiplexer
I/O Control 230
RAM look-up with
64-to-1 multiplexer
190
To timing
and
formatting
sub-systems

FIG. 3

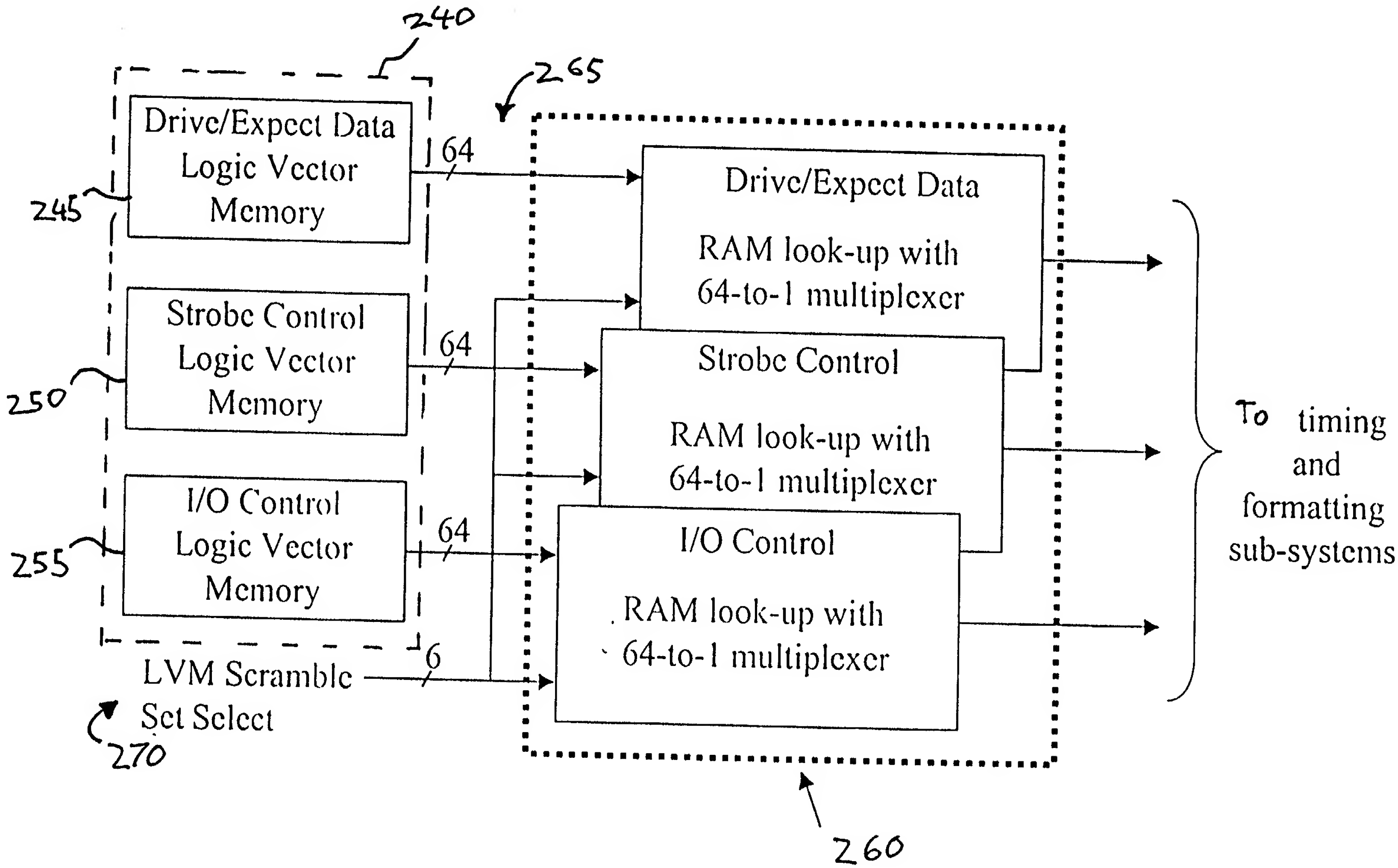
240
265
Drive/Expect Data
Logic Vector
Memory
245
Strobe Control
Logic Vector
Memory
250
I/O Control
Logic Vector
Memory
255
LVM Scramble
Set Select
270
64
64
64
6
Drive/Expect Data
RAM look-up with
64-to-1 multiplexer
Strobe Control
RAM look-up with
64-to-1 multiplexer
I/O Control
RAM look-up with
64-to-1 multiplexer
260
To timing
and
formatting
sub-systems

FIG. 4

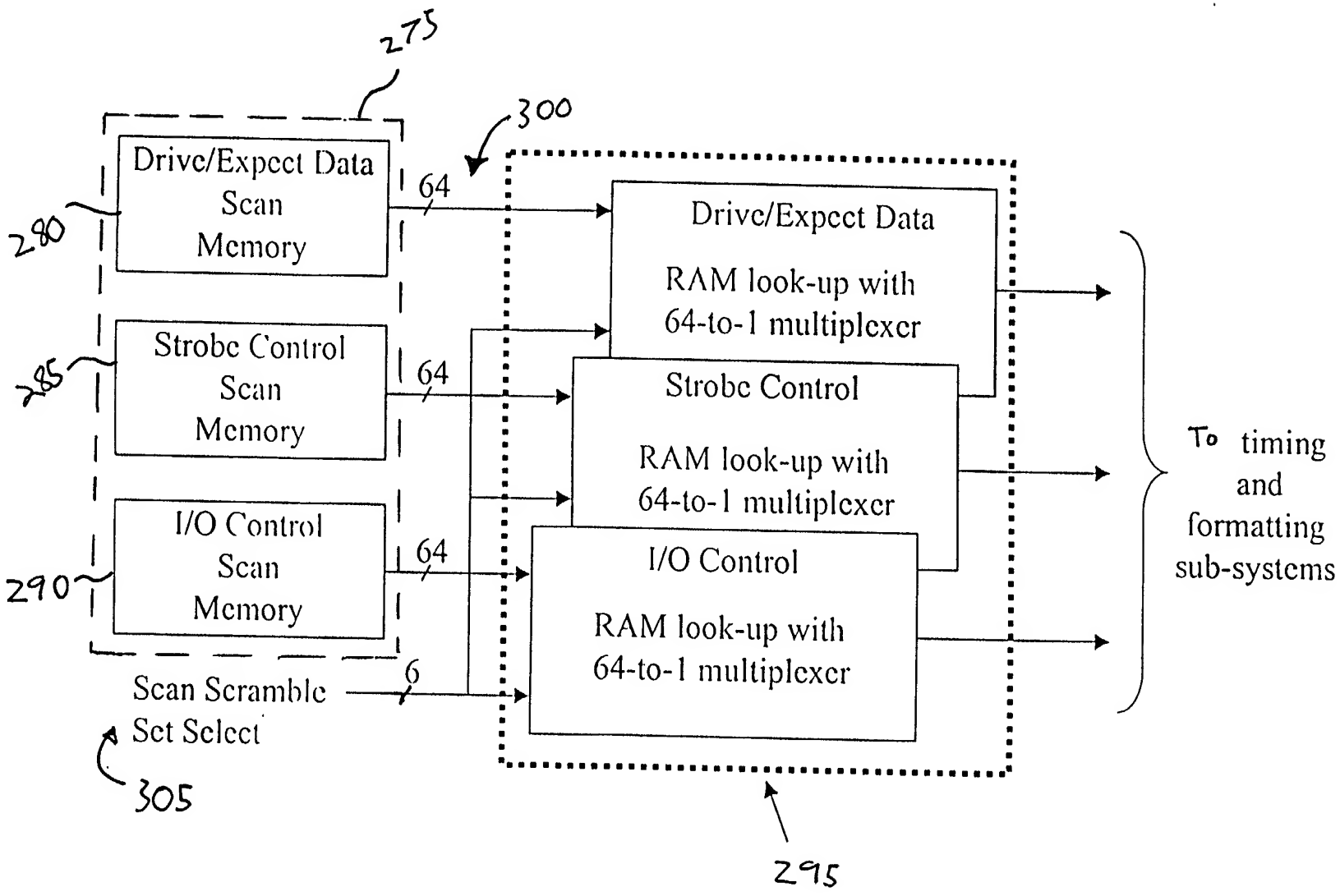

FIG. 5

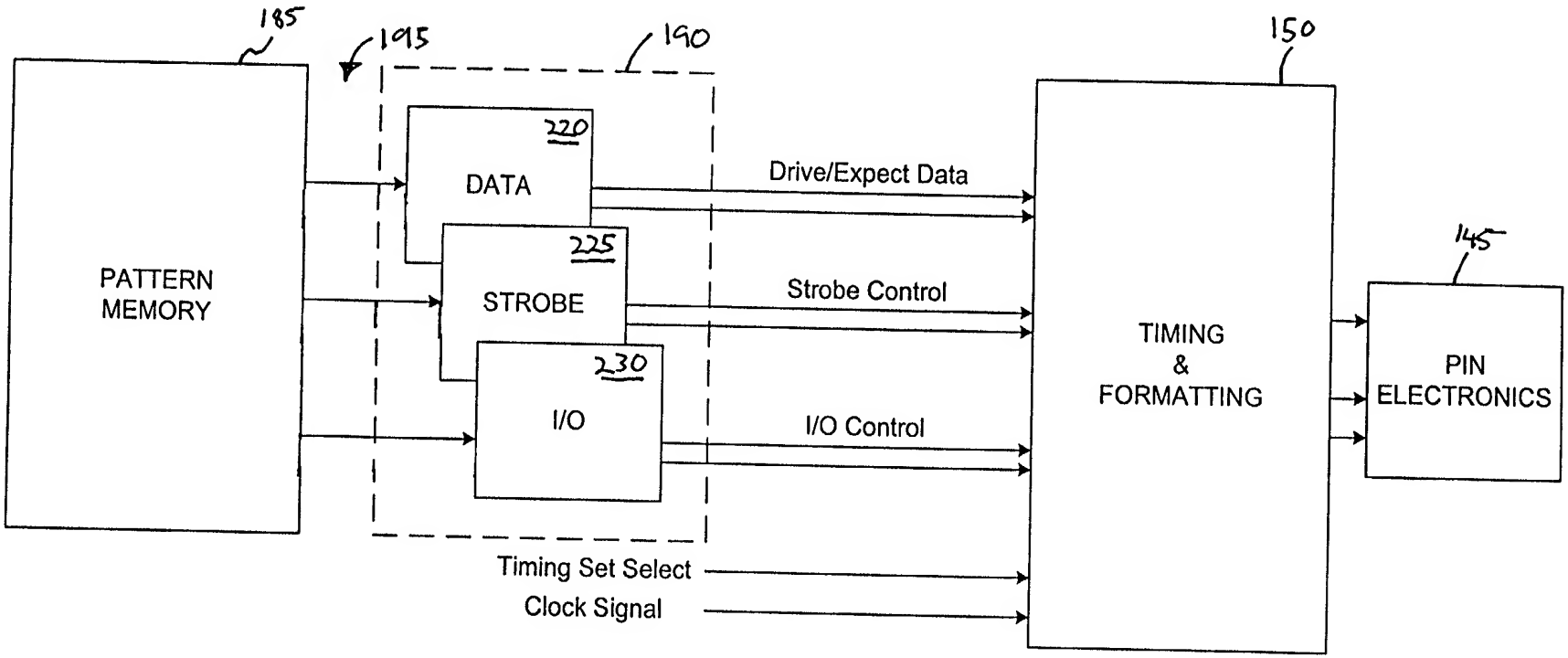

Fig. 6

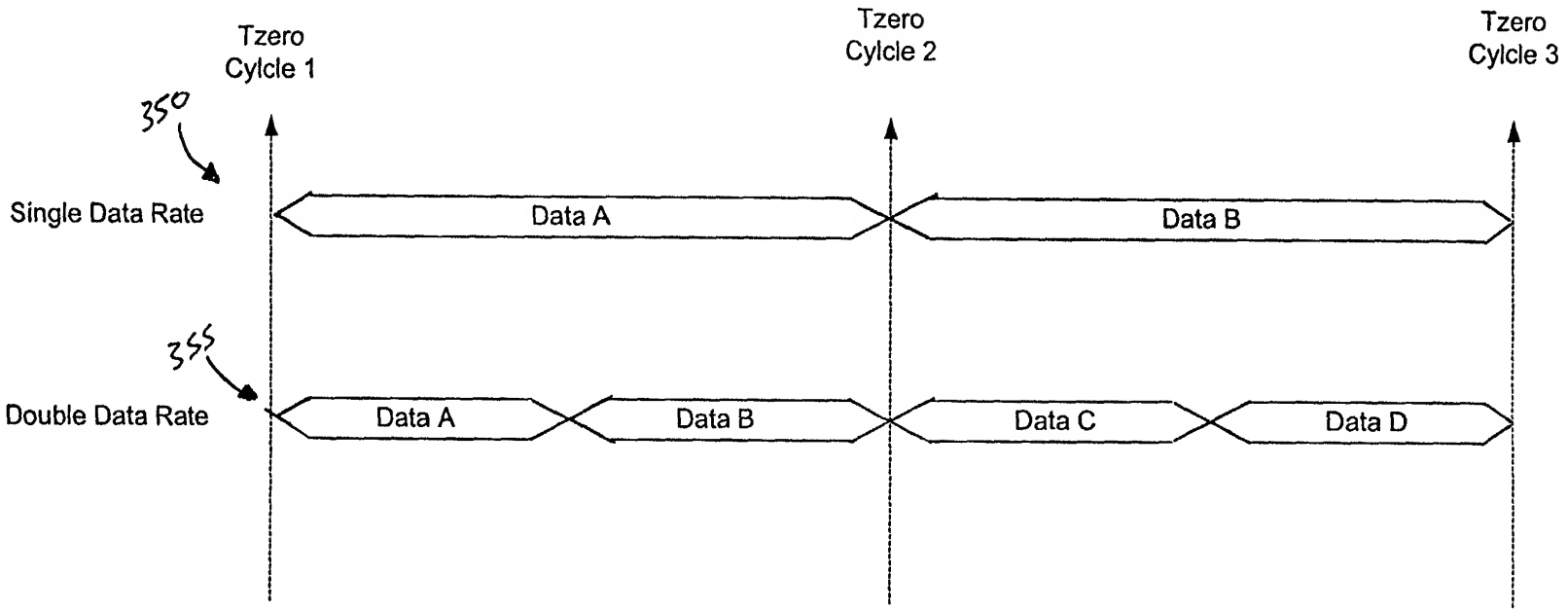

Fig. 7

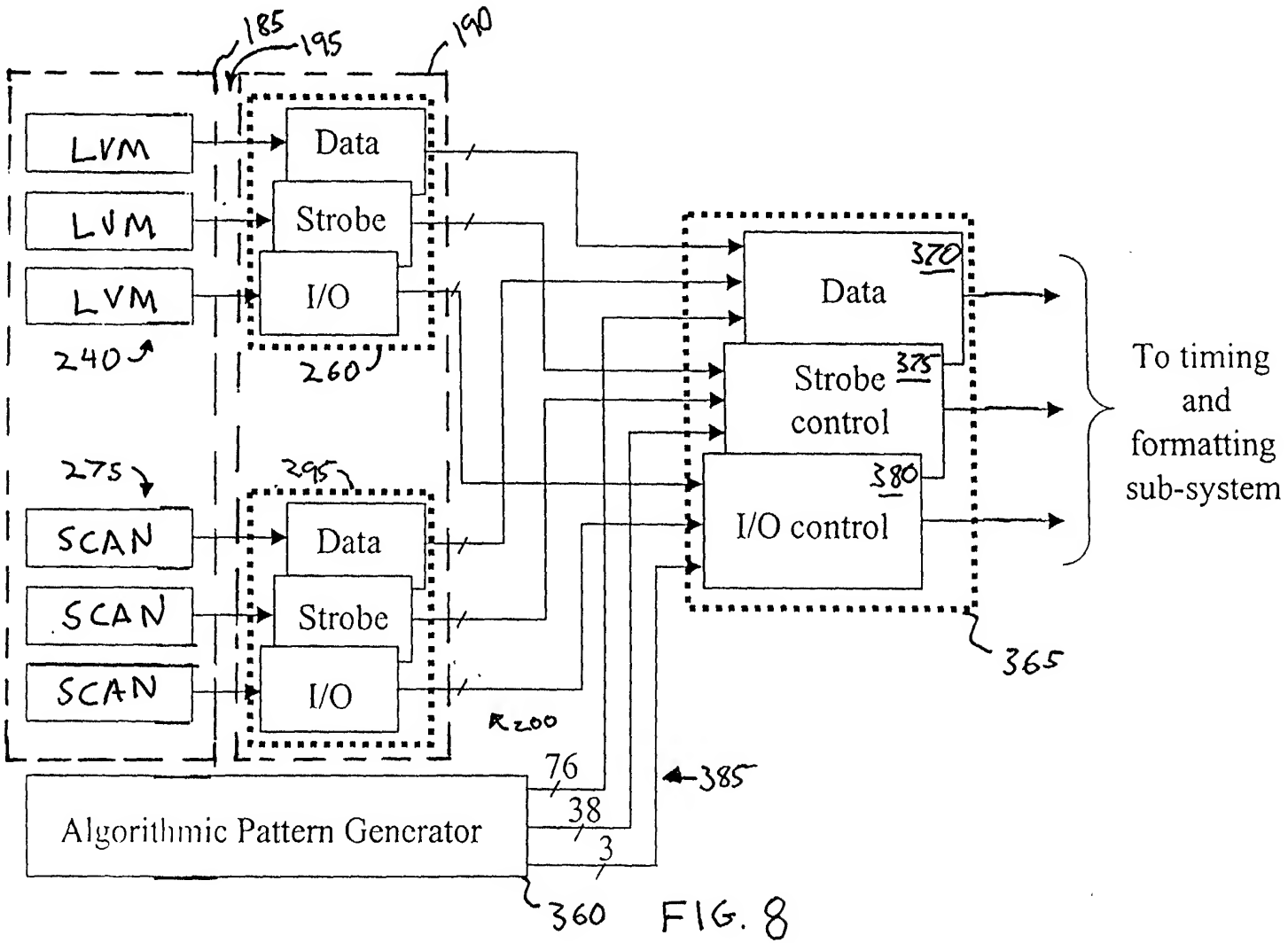
185
195
190
LVM
LVM
LVM
240
Data
Strobe
I/O
260
275
295
SCAN
SCAN
SCAN
Data
Strobe
I/O
R200
370
Data
375
Strobe control
380
I/O control
365
To timing and formatting sub-system
76
38
3
385
Algorithmic Pattern Generator
360

FIG. 8

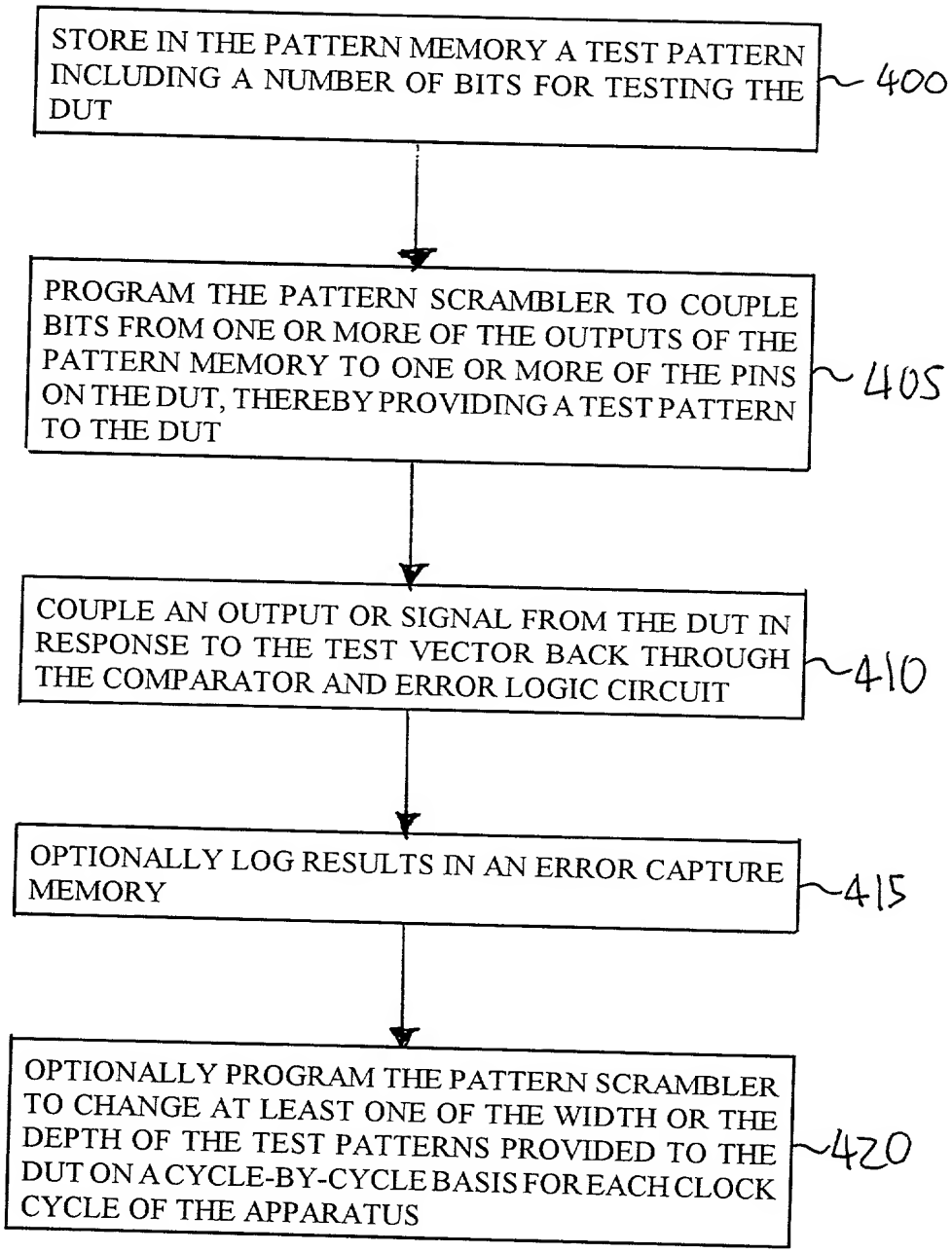
STORE IN THE PATTERN MEMORY A TEST PATTERN INCLUDING A NUMBER OF BITS FOR TESTING THE DUT
400
PROGRAM THE PATTERN SCRAMBLER TO COUPLE BITS FROM ONE OR MORE OF THE OUTPUTS OF THE PATTERN MEMORY TO ONE OR MORE OF THE PINS ON THE DUT, THEREBY PROVIDING A TEST PATTERN TO THE DUT
405
COUPLE AN OUTPUT OR SIGNAL FROM THE DUT IN RESPONSE TO THE TEST VECTOR BACK THROUGH THE COMPARATOR AND ERROR LOGIC CIRCUIT
410
OPTIONALLY LOG RESULTS IN AN ERROR CAPTURE MEMORY
415
OPTIONALLY PROGRAM THE PATTERN SCRAMBLER TO CHANGE AT LEAST ONE OF THE WIDTH OR THE DEPTH OF THE TEST PATTERNS PROVIDED TO THE DUT ON A CYCLE-BY-CYCLE BASIS FOR EACH CLOCK CYCLE OF THE APPARATUS
420

FIG. 9